classifying said defect from said feature;

irradiate said defect on said circuit pattern again after classifying said defect; and

displaying an SEM image of said defect extracted from the result of said comparison after said classifying step formed by said step of irradiating again.

4. (Amended) An inspection apparatus for a circuit pattern, comprising;

a first apparatus of a first type including:

an electron source for generating an electron beam;

an electronic optical apparatus which is constructed by a plurality of electronic lenses and irradiates said electron beam onto a surface of a substrate on which a circuit pattern has been formed;

a detector for detecting a signal which is generated from said substrate by said irradiation;

a defect extracting apparatus for visualizing the signal detected by said detector as an image and extracting a defect on said circuit pattern;

a second apparatus of a second type for examining and extracting the defect from the same circuit pattern;

a monitor for displaying, in overlapping manner, a first image of the defect extracted by said defect extracting apparatus, and a second image of the same defect obtained from said second apparatus.

REMARKS

Claims 1-5 and 9-12 are pending in this application. Claims 2 -4 have been amended to better bring out features of Applicants' invention.

Claims 1 and 10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,578,821 to Meisberger et al. in view of U.S. Patent No. 6,259,960 to Inokuchi and U.S. Patent No. 6,263,099 to Maeda et al. Claims 2 and 3 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Meisberger et al. Claims 4, 5 and 11 stand rejected under 35 U.S.C.

103(a) as being unpatentable over Meisberger et al. in view of U.S. Patent No. 4,091,374 to Muller et al. and Inokuchi. Finally, claims 9 and 12 stad rejected under 35 U.S.C. 103(a) as being unpatentable over Inokuchi in view of U.S. Patent No. 5,973,777 to Nomoto et al. Applicants' respectfully traverse these rejections and believe that the claims clearly define over the art.

A significant limitation in Claims 1 and 10 is the designation of a size of pixel in accordance with the width of the circuit pattern. It is the Examiner's position that Inokuchi discloses that "the magnification is adjusted so that the foreign material or defect portion assumes an appropriate size on the display screen." The Examiner then states that Maeda teaches an image magnification that is related to the pixel size of a detected image. The Examiner concludes that, since defects are smaller than the width of the circuit pattern, it would be obvious to adjust the magnification of the image of the defects in accordance with the width of the circuit pattern.

However, claims 1 and 10 do not define a relation between the magnification of the image and the pixel size. These claims require that the pixel size be determined on the basis of a size of the circuit pattern to be inspected, i.e., on the basis of the line width of the circuit pattern. This feature is clearly defined in claims 1 and 10. No reference alone discloses this, nor can one reach what is claim by combining the references. Thus, claims 1 and 10 should be allowed.

Claims 2 and 3 have as a significant limitation displaying an SEM image of defects after classifying the defects. It is the Examiner's view that Meisberger teaches that the results of the classification are fed to the system computer which sends signals to the image display 46. The signals are also stored in memory block 52. The Examiner concludes that it would have been obvious to those skilled in the art to display the stored image signals at any point including after the defect classification.

Claims 2 and 3 have been amended to more clearly define the manner of displaying the SEM image after classifying, making what was implicit explicit. (Note, for example, in claim 2, prior to amendment the limitation "the SEM image obtained by irradiating again.") As amended, Applicants submit that the invention defined in amended claims 2 and 3 now clearly distinguishes over Meisberger. This reference does not teach irradiating again to obtain an SEM image after classifying.

The last paragraph of claim 4 defines displaying, in parallel, a first image of the defect extracted by the defect extracting apparatus and a second image of the same defect obtained from another apparatus. Meisberger discloses displaying an SEM image on a monitor. Muller discloses displaying, simultaneously and in parallel, an image of a defect and an image in which a part of the defect is magnified, on individual monitors. Inokuchi discloses that an image of the defect or defect information is transmitted from another apparatus.

Accordingly, the Examiner believes that it would have been obvious to those skilled in the art, by combining the above three cited references, to display, simultaneously and in parallel, the image of the defect and the image of the same defect transmitted from the other apparatus, on individual monitors, and further it would be obvious to replace the display using separate monitors by a display of a single monitor. In the first instance Applicant's do not believe that the Examiner has pointed to sufficient motivation to make all of these modifications. Only in hindsight, with Applicant's specification to point the way can one reach the claimed invention.

Furthermore, none of the cited references discloses displaying an image of a defect and an image of the same defect transmitted from the other apparatus, in an overlapping manner as now brought out in claim 4. (Claim 4 has been amended to clarify what is intended by "in parallel.") By doing so, even if an image from one of the apparatuses is not clear, if an image from another apparatus is clear, the inspection of a circuit pattern of higher precision can be carried out (refer to the first paragraph on page 71, paragraph 294). Thus, this claim is also allowable.

The invention defined in claims 5 and 11 includes the features of displaying a wafer map, an electron beam image of the defect and defect information. Meisberger discloses comparing an image of a defect with an image transmitted from an external apparatus or a database. Muller discloses to simultaneously displaying a real time image and an image from another inspection apparatus. Inokuchi discloses receiving defect information or an image transmitted from another apparatus. Based on all of this, the Examiner considers that it would be obvious to display, simultaneously and in parallel, an image of a defect and an image of a defect or defect information transmitted from another apparatus.

Applicants note that the Examiner does not refer to a display of a wafer map. In fact, no cited reference discolored displaying a wafer map. Therefore, the teachings of these references cannot make it obvious to simultaneously display the wafer map, the image of defect and the defect information.

An important point of the invention claimed in claims 9 and 12 is to detect a position at which a defect exists, using a marking established at a position *near* to the position of the defect. It is the Examiner's view that Inokuchi teaches using alignment marks on a wafer. Nomoto teaches that such marks can be written on a substrate near a defect by the inspection apparatus when a defect is discovered. The Examiner then contends that it would have been obvious to those skilled in the art to use Nomoto's marking apparatus to provide the alignment marks required by Inokuchi.

The Examiner's characterization of Nomoto is incorrect. Nomoto discloses, in lines 3-8 on column 6, that "the stage controller 21 moves the marking unit 12 to the location of the surface-shape defect . . . ." The location is then marked with something that allows the surface-shape defect to be seen with ease. That is to say, the Nomoto discloses making a marking *at* the location of the surface-shape defect. It is to be noted that the Nomoto does not disclose establishing the marking at a location *near* to a position of the defect.

Nomoto has as its object the detecting of a position of a defect such as a deformation/irregularity on the surface of a plane member. Accordingly, no problem arises in Nomoto if the marking is made on the defect itself and the marking position indicates the position at which the defect exists.

On the other hand, in the present invention, the problem to be solved is that it is difficult to put a mark at a position of defect itself, since such a defect is very small in a semiconductor substrate, to which the present invention is directed. Therefore, in the present invention, a mark is established at a location near to a position of the defect. As a result, the defect can be easily found using the marking as a guide. In other words, following the teaching of Nomoto, one does not reach the claimed invention. Thus, these claims too should be allowed.

In view of the above, entry of this amendment is proper; the minor changes made only bring out what was already in the claims amended and place them in condition for allowance or better form for appeal. In fact, the discussion above shows that with entry of this amendment all claims in this application will be in condition for allowance. Thus, entry of this amendment and prompt notice of which is respectfully solicited.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"Version With Markings To Show Changes Made."**

The Examiner is invited to call the undersigned at (202) 220-4200 to discuss any information concerning this application.

Applicants respectfully request a three month Extension of Time to respond to the Office Action of May 30, 2002. The extended period expires December 2, 2002 (November 30th falls on a Saturday).

"Version With Markings To Show Changes Made"

IN THE CLAIMS:

Amend claims 2, 3 and 4 as indicated below:

2. (Amended) An inspection apparatus for a circuit pattern, comprising:

an irradiating apparatus which is constructed by a plurality of lenses and irradiates light, a laser beam, or a charged particle beam onto a surface of a substrate on which a circuit pattern has been formed;

a detector for detecting a signal which is generated from said substrate by said irradiation;

a memory for storing the signal obtained by said detector and visualized as an image, said memory storing an SEM image which is obtained by irradiating said charged particle beam only once to one region on the surface of said substrate;

a comparing apparatus for comparing said signal stored in said memory with a signal obtained by visualizing a corresponding comparison pattern in another region as an image;

a monitor for displaying a defect on said circuit pattern from a result in said comparing apparatus;

a defect classifying apparatus for extracting a feature of the defect on said circuit pattern included in said SEM image and classifying said defect; and

a processor programmed to cause said irradiating apparatus to irradiate said defect on said circuit pattern again after classifying said defect, and to cause said monitor to selectively display an image of the defect on said circuit pattern obtained from a result in said comparing apparatus or the SEM image obtained by irradiating again said charged particle beam to said defect on the basis of a result of the classification in said defect after classifying in said defect classifying apparatus classifying apparatus.

3. (Amended) An inspection method for a circuit pattern, comprising the steps of:

forming an SEM image by irradiating a charged particle beam only once to one region on a surface of a substrate on which a circuit pattern has been formed;

detecting a signal which is generated from said substrate by said irradiation;

storing a signal obtained by said detection and visualized as an image;

comparing said stored signal with a signal obtained by visualizing a corresponding comparison pattern in another region as an image;

extracting a defect on said circuit pattern from a result of said comparison;

extracting a feature of said defect included in said SEM image;

classifying said defect from said feature;

irradiate said defect on said circuit pattern again after classifying said defect; and

displaying [said] an SEM image of said defect extracted from the result of said comparison after said classifying step formed by said step of irradiating again.

4. (Amended) An inspection apparatus for a circuit pattern, comprising;

a first apparatus of a first type including:

an electron source for generating an electron beam;

an electronic optical apparatus which is constructed by a plurality of electronic lenses and irradiates said electron beam onto a surface of a substrate on which a circuit pattern has been formed;

a detector for detecting a signal which is generated from said substrate by said irradiation;

a defect extracting apparatus for visualizing the signal detected by said detector as an image and extracting a defect on said circuit pattern;

a second apparatus of a second type for examining and extracting the defect from the same circuit pattern;

a monitor for displaying, in [parallel] overlapping manner, a first image of the defect extracted by said defect extracting apparatus, and a second image of the same defect obtained from said second apparatus.

The Office is hereby authorized to charge the fee of $920.00 for a Petition for Extension of Time Under 37 C.F.R. § 1.136(a) and any additional fees under 37 C.F.R. § 1.16 or § 1.17 or credit any overpayment to Deposit Account No. 11-0600.

Respectfully submitted,

Dated: December 2, 2002

John C. Altmiller
Registration No. 25,951

KENYON & KENYON
1500 K Street, N.W., Suite 700
Washington, D.C. 20005-1257
Tel: (202) 220-4200
Fax: (202) 220-4201